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09/266,869	03/12/1999	KAZUYA TANIGUCHI	P8075-9008	6342

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EXAMINER
PATEL, GAUTAM

ART UNIT	PAPER NUMBER
2655	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/266,869	Applicant(s) Taniguchi et al.
	Examiner Gautam R. Patel	Art Unit 2655

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 7, 2002* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-14, 16-18, and 24-34* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14, 16-18, and 24-34* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Response to Amendment

1. This is in response to amendment filed on 10-7-02 (Paper # 15).

2. Claims 1-14, 16-18 and 24-34 remain for examination. Claims 24-34 are newly presented for examination.

3. Applicant's arguments regarding rejection of claims 1-18 under 35 U.S.C. § 112 second paragraph have been fully considered and rejection of claims 1-18 under 35 U.S.C. 112 second paragraph has been **withdrawn**. However new 112 second rejection follows on new claims.

Claim Objections

4. Claims 3, 26, 29, 31 and 33 are objected for following reasons.
   a. Claim 3, line 2 "buffers connected in parallel with the memory," is confusing and unclear. May be "buffers connected in parallel to the memory," may convey the meaning better. Since buffers are connected in parallel to memory as shown in fig. 1.
   b. Claim 26, lines 1-3 "counting the address for at least one instruction or the address for data so that the second unit skips the pseudo instruction." is confusing and unclear. How can counting address could the skip the pseudo instruction.
   c. Claims 29, 31 and 33 have similar problems.

Perhaps wording like "incrementing the address for at least one instruction or the address for data so that the second unit skips the pseudo instruction" may make more sense and convey the idea better.

Corrections and/or explanations are required.

Claim Rejections - 35 U.S.C. § 112

5. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 24-25 and 27-28 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claim 24, lines 1-3 "the pseudo instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data instruction." is confusing and unclear. Since specification discloses that program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction. [page 2-3; specification]. In other words these are different instructions. Specification teaches **opposite** of what is being claimed. That these instructions are separate and distinct, and specification in other places supports these lines. Also careful examination of page 7, page 18 and page 25 does not disclose this aspect at all that pseudo instruction itself is branch instruction or call instruction.

b. Claim 24, lines 1-3 the scope of " the pseudo instruction is one of an unconditional branch instruction ... " lacks proper antecedent basis in the specification.

c. Similarly claim 27 has same problem as claim 24.

d. Claim 25 lines 1-2 "executing a no-operation (NOP) instruction in accordance with a detection of the pseudo instruction." lacks proper antecedent basis. No place in specification including page 7, page 18 and

page 25 describes that a NOP instruction is executed when the pseudo instruction is detected.

e. Claim 28 has similar problem as claim 25. No antecedent basis for that concept.

f. Claim 30 has similar problem as claim 25. Also claim 30 line 10 "executing a no-operation (NOP) operation" is confusing. NOTE: It is assumed that typographical error wad made and "(NOP) instruction" was meant instead of (NOP) operation.

Claim Rejections - 35 U.S.C. § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 6-8, 16-18, 30, 32 and 34 are rejected under 35 U.S.C. § 102(b) as being anticipated by Cocke et al., US. patent 3,577,189 (hereafter Cocke).

As to claim 1, Cocke discloses the invention as claimed [see Figs. 1-7A; especially fig. 5] including detecting pseudo instruction and arranging it before one instruction reading a program, reading data. Storing instruction or data and executing data, comprising the steps of:

a. reading the program from the memory [storage system; col. 5, lines 21-23] [col. 1, line 73 to col. 2, line 45];

b. detecting the pseudo instruction [branch instruction; fig. 5, instruction after Opa3] with a first unit [fig. 1A, unit 8] [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5];

c. reading the instruction or data in accordance with the address for the instruction or the address for the data with the first unit [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5];

d. storing the instruction or the data in a buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5]; and

e. executing the stored instruction with a second unit [execution unit] [col. 1, line 73 to col. 2, line 45]. (NOTE: Execution unit is inherently present in any computer system and is inherently separate from predecode unit.)

NOTE: As it has been pointed out by the Examiner that "prepare to branch" and related concepts are well known in the art for a very long time. The vocabulary is slightly different in old patents. Cocke's so called "branch instruction" works as a pseudo instruction and Cocke's so called "exit instruction" is actually a branch instruction in today's vocabulary

7. As to claim 2, Cocke discloses:

a pseudo instruction [branch instruction] detection unit [Fig. 1A, unit 8] connected with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit in parallel [see lines 6 and 10 in fig. 1A] with the buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

8. As to claim 6, Cocke discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction or data from the memory in accordance with the at least one instruction address or data address with the first unit after the transfer of the at least one instruction to the first buffer has been identified [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

9. As to claim 7, Cocke discloses:

Identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address with the first unit when the pseudo instruction is detected wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

10. As to claim 8, Cocke discloses:

a buffer [fig. 1A, unit 2], connected to a memory ["storage system"; col. 5, lines 21-23], for storing instructions and data of a program read from the memory, wherein the program includes a pseudo instruction [branch instruction; fig. 5, instruction after Opa3], and at least one instruction [fig. 5, OPa4], the pseudo instruction being arranged before the at least one instruction and including an address for the at least one instruction or an address for data [col. 1, line 73 to col. 2, line 75 and col. 3, lines 36-54];

a first unit including,

a pseudo instruction detection unit [fig. 1A, unit 8], connected to the memory, for detecting the pseudo instruction included in the program read from the memory;

an address control unit [inherently present, since Cocke is calculating addresses], connected to the external memory and the pseudo instruction detection unit, for reading the instruction or data in accordance with the address for the data and storing the instruction or data in the buffer [col. 1, line 73 to col. 2, line 45]; and

a second unit [execution unit] connected to the buffer, for executing the instruction [col. 1, line 73 to col. 2, line 45] stored in the buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5]. NOTE: Since Cocke is executing instructions execution unit is inherently present.

11. As to claim 15 it is rejected for the same reasons set forth in the rejection of claim 1, supra.

As to added limitation of the recording medium having program stored in them [col. 5, lines 21-23; "storage system"].

12. As to claim 16, it is rejected for the same reasons set forth in the rejection of claim 1 and 8, supra.

As to the added limitation of

a bus [fig. 1, unit 6] interconnecting the prefetch buffer [fig. 1, unit 8] and the memory [storage system; col. 5, lines 21-23].

A holding circuit [fig. 1A, unit 2].

13. As to claim 17, Cocke discloses:

the pseudo instruction detection unit further comprises:

a pseudo instruction detection circuit that receives at least a part of each of the instructions and data being transferred from the memory to the prefetch buffer, detects an opcode of a pseudo instruction therefrom, and generates a detection signal; and

a shift register [fig. 1A, unit 2 and ROW 0, 1, 2 etc works as shift register as they are pushing instructions down from one level to next; see col. 10, lines 67-75] connected to the pseudo instruction detection circuit and receiving the detection signal, and generating a hold circuit enable signal, wherein when the hold
circuit enable signal is active, the holding circuit stores the pseudo instruction operands being transferred on the bus [col. 4, lines 49-75].

14. As to claim 18, Cocke discloses:

an additional information holding circuit that stores a first operand [fig. 1A, ROW 0, block "I"] of the pseudo instruction;

an upper address holding circuit that stores a second operand [fig. 1A, ROW 0, block "J"] of the pseudo instruction; and

a lower address holding circuit that stores a third operand [fig. 1A, ROW 0, block "K"] of the pseudo instruction, wherein the second and third operands comprise a memory address [col. 4, lines 49-75 especially 64-68].

15. As to claim 30 it is rejected for the same reasons set forth in the rejection of claims 1 and 6, supra.

16. As to claim 32 it is rejected for the same reasons set forth in the rejection of claim 1 and claim 25, supra.

17. As to claim 34 it is rejected for the same reasons set forth in the rejection of claim 1, supra.

Claim Rejections - 35 U.S.C. § 103

18. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 3-5, 9-14, 23, 26, 29, 31 and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cocke as applied to claims 1-2, 6-8, 16-18, 30, 32 and 34 above.

20. As to claim 3 Cocke discloses:

. the buffer includes first [fig. 1A, unit 2, sub-unit ROW N] and second [fig. 1A, unit 2, sub-unit ROW 0] buffers connected, and the method further comprising a step of storing, the instruction and data read from the memory in the first buffer and storing the instruction or data included in the detected pseudo instruction in the second buffer [col. 5, lines 17-48 and col. 7, lines 38-50];

Cocke does not teach that the buffers are connected in parallel with the memory. However it would have been obvious to a person of ordinary skill at the time of the invention to have placed the buffer and detection unit in parallel and put them into the system of Cocke because doing so would make design more faster. As shown in "In re Japikse **86 USPQ 70 (CCPA 1950)**", to rearrange parts for different storage method is generally not given patentable weight or would have been obvious improvements.

21. As to claim 4, Cocke discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with first unit when the pseudo instruction is detected [fig. 5 and col. 10, line 56 to col. 11, line 34]; and

prefetching the instruction or data from the memory [col. 3, lines 36-54] in accordance with the at least one instruction address or data address with the first unit after the transfer of the at least one instruction to the first buffer has been identified [col. 1, line 73 to col. 2, line 75].

22. As to claim 5, Cocke discloses:

Identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer [col. 1, line 73 to col. 2, line 75 and col. 3, lines 36-54].

23. As to claim 9, it is rejected for the same reasons set forth in the rejection of claim 3, supra.

24. As to claim 10, Cocke discloses:

the address control unit identifies that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected and permits storage of the instruction or data in the second buffer when the corresponding instruction or data is not stored in the second buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

25. As to claim 11, it is rejected for the same reasons set forth in the rejection of claim 2, supra.

26. As to claim 12, it is rejected for the same reasons set forth in the rejection of claim 10, supra.

27. As to claim 13, it is rejected for the same reasons set forth in the rejection of claim 11, supra.

28. As to claim 14, Cocke discloses:

a detection circuit [Fig. 1A, unit 8], connected to a data line [fig. 1, unit 6 and unit 10], for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5]; as to the rest of the claim

Cocke does not disclose a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit

supplies a signal for validating the opcode detection operation during an operand transfer period. "Official Notice" is taken that both the concept and the advantages of providing a detection timing circuit which can calculate transfer period based on the instruction length and number of operands are well known. It would have been obvious to provide a timing circuit to Cocke' system as this circuit is known to provide the system with a timing estimate and send valid operand into the system. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

29. As to claims 26 and 29, Cocke does not disclose that the second unit [execution unit] skips the pseudo instruction and executes the prefetched instruction. However one of ordinary skill in the art at the time invention would have realized that computer time and resources are at premium and it would be unwise and useless to execute an instruction that is not producing any results in the execution unit. One would have been motivated to make system faster by not performing unnecessary tasks.

Therefore it would have been obvious to have skipped the execution of the pseudo instruction in the system of Cocke because it would have saved time and resources during execution by not executing unnecessary instruction.

30. As to claims 31 and 33, they are rejected for the same reasons set forth in the rejection of claim 30, supra. As to the added limitations:

Cocke does not disclose the added limitation of second unit [execution unit] skips the pseudo instruction and executes the prefetched instruction. However one of ordinary skill in the art at the time invention would have realized that computer time and resources are at premium and it would be unwise and useless to execute an instruction that is not producing any results in the execution unit. One would have been motivated to make system faster by not performing unnecessary tasks thus saving computer time.

Therefore it would have been obvious to have skipped the execution of the pseudo instruction in the system of Cocke because it would have saved time and resources during execution by not executing unnecessary instruction.

31. Applicant's arguments with respect to claims 1-14, 16-18 and 24-34 have been considered but are deemed to be moot in view of the new grounds of rejection.

Allowable Subject Matter

32. Claims 17 and 18 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other prior art cited

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Schlansker et al. (US. patent 5,664,135) "Apparatus ans method for reducing delays due to branches".
    b. Grochowski et al. (US. patent 5,442,756) "branch prediction and resolution apparatus for a superscalar computer processor".
    c. Misaka (US. patent 5,050,076) "Prefetching queue control system".
    d. Sturges et al. (US. patent 5,961,637) "Split branch system utilizing separate set branch, condition and branch instructions and including dual instruction fetchers".
    e. Watson et al. (US. patent 3,573,854) "Look-ahead control for operation of program loops".
    f. Emma et al. (US. patent 4,991,080) "Pipeline processing apparatus ...".

34. Applicant's amendment necessitated the new grounds of rejection presented in this office action. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact information

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ms. Doris To can be reached on (703) 305-4827.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

GRP

RICHARD L. ELLIS
PRIMARY EXAMINER

Gautam R. Patel
Patent Examiner
Group Art Unit 2655

November 12, 2002